REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1-5, 7-13, 15-18 and 20 are in the case. Claims 6, 14 and 19 are canceled. No amendments have been made.

Regarding the rejection of Claims 1, 8, 15, and 20 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the patent to Maemura in view of the patent to Miyake or the patent to Yoshioka, this rejection is respectfully traversed. Claims 1 and 8 recite a program counter copy register for storing a program memory address pointed to by a program counter as a return address from a debug monitor routine, while Claim 15 recites the step of storing a memory address in a program counter copy register, wherein the address is reloaded into a program counter after execution of a debug routine.

As discussed in the previous amendment, these elements, which are neither shown nor suggested in the patent to Maemura, provide an important way for returning to the normal user program after executing a debug routine. Under normal conditions, a program counter copy register as recited may be operated to be continuously updated, for example with a current instruction fetch address. When a breakpoint occurs, the program counter copy register may then be locked, thereby storing the match instruction address. A long jump instruction may then be inserted to run the debug routine. At the end of the execution of the debug routine is finished, a return instruction may be executed, and the address stored in the program counter copy register used as the resume address. In this way, resumption of the normal program is assured. An additional benefit is that the program memory may be accessed during execution of the debug routing. This allows, for example, microprocessor execution condition information stored in the program memory to be outputted during debug.

By contrast, the patent to Maemura fails to even mention how to return to the breakpoint address and continue normal user program execution. The

comments on Maemura made in the previous Amendment are still relevant, and are incorporated here by reference as if set forth in their entirety. In addition, it is noted that it has been admitted that Maemura does not teach a program counter, and that Maemura does not teach storing of the program counter address in a register as a return address from a debug routine so after the debug is finished the system can return to the program at the proper location. However, it is alleged that this is taught in Miyake and in Yoshioka. This allegation is respectfully disputed.

Regarding Miyake, in column 15, lines 7 – 16, program counter ("PC") next address sources are discussed. In the normal case, the PC is just incremented from the previous value, otherwise it comes from branch destination address 474, or interrupt return address 475, or normal interrupt handler start address 476, or break interrupt handler start address 477. None of this relates to what is recited in Claims 1, 8 and 15. According to these claims only the program memory address pointed to by the program is stored as a return address, so that a RET instruction (return from interrupt) may be used to change to a new PC value in microprocessor. This claimed aspect may thus be under monitor program control. The PC copy register provides the monitor program capability to return to interrupted address. It advantageously does not require the use of hardware to change PC value. It uses the general microprocessor return from interrupt or subroutine mechanism to change the PC value.

Further, in column 15, lines 17 -27, Miyake's break interrupt is triggered by the instruction read out from memory 410. The instruction fetch controller 421 decodes incoming instruction 472 to decide if it detects a break interrupt. It decodes the fetched instruction to determine break interrupt detection, which is equivalent to detecting an illegal instruction code. According to Claims 1, 8 and 1, the value in the program counter is simply compared against a breakpoint address to determine that a breakpoint has occurred.

Still further, in Miyake, at column 15, line 66 – column 16, line 23, and column 17, lines 1-30, his arrangement compares the fetched instruction code

for an illegal instruction (such as division by zero or data overflow) and it does not compare the instruction memory address. Its break interrupt or normal interrupt functions are used to detect an illegal instruction. The invention as set forth in Claims 1, 8 and 15 is used to debug an application program during a development phase. It is not intended to detect illegal instruction codes. It does not save registers in hardware for return from interrupt. The PC copy register is simply used to keep the current breakpoint address for return from a monitor program, and microprocessor other register recovery is handled by software, which may use the stack push/pop operation to save and recover microprocessor internal register values. This allows for software implementation for microprocessor internal register value recovery. Miyake's invention uses a hardware implementation for microprocessor internal register value recovery.

Regarding Yoshioka, while it mentions in column 9, lines 21-41 a breakpoint address register, there is no teaching or suggestion on how the microprocessor is to decide that a breakpoint condition might be met. Further, while saving the current PC value is mentioned in column 10, lines 30-47, and that the instruction pointed to by the saved PC value will be executed after return from the exception handler, when the saved PC value instruction is executed, the breakpoint condition is met again and a break interrupt loop will occur as in Maemura's arrangement. Thus, as in Maemura, what is taught in this reference is not operable. Further, Yoshioka cryptically states, The saved program counter SPC stores values of the program counter PC at predetermined timings if an exception event occurs." (Column 10, lines 39-41.) There is no teaching or suggestion as to what such "predetermined timings" are, or when or how they would be known to occur.

Thus, the recited elements in Claims 1, 8 and 15 provide an important function that is neither shown nor suggested by the patent to Maemura, and, further, the patents to Miyake and to Yoshioka fail to cure the deficiencies of Maemura.

The other art of record is even less relevant. It is therefore respectfully submitted that for the above reasons independent Claims 1, 8 and 15 are allowable over Maemura and, indeed, all of the art of record, either considered alone or in any combination. Claim 20 depends from Claim 15, and so is allowable for the same reasons, as well as for the additional limitations found therein. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

Regarding the rejection of Claims 2, 3, 5, 10, 11, 13, 16, 17 and 18 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the patent to Maemura in view of the patent to Yishay et al., this rejection is respectfully traversed.

The reasons for the allowability of independent Claims 1, 8 and 15 over the patent to Maemura are set forth above. The patent to Yishay et al. fails to cure the deficiencies of the patent to Maemura, apparently relating to comparison logic for breaking an address signal 54 into upper address signals and lower address signals. It fails to teach or suggest how to enter a breakpoint routine or how to return from it. In addition, it fails to teach or suggest the additional limitations found in these dependent claims. It is therefore respectfully submitted that Claims 1, 8 and 15 are allowable over Maemura and Yishay et al. Claims 2, 3 and 5 depend, directly or indirectly from Claim 1, Claims 10, 11 and 13 depend, directly or indirectly from Claim 8 and Claims 16, 17 and 18 depend, directly or indirectly from Claim 15, and so all are allowable for the same reasons, as well as for the additional limitations found therein. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

Regarding the rejection of Claims 4, 9 and 12 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the patent to Maemura in view of the patent to Favor, this rejection is respectfully traversed. The reasons for the allowability of Claims 1 and 8 over the patent to Maemura are set forth above. The patent to Favor fails to cure the deficiencies of the patent to Maemura, apparently relating to an Intel x86 type instruction set translator, and having apparently nothing to do with single step breakpoint traps. In addition, it fails to teach or suggest the

additional limitations found in these dependent claims. It is therefore respectfully submitted that Claims 1 and 8 are allowable over Maemura and Favor. Claim 4 depends from Claim 1 and Claims 9 and 12 depend from Claim 8, and so all are allowable for the same reasons, as well as for the additional limitations found therein. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

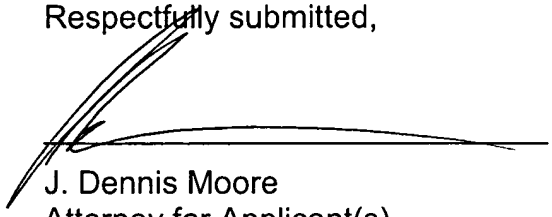
Regarding the rejection of Claim 7 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the patent to Maemura in view of the patent to Jaggar, this rejection is respectfully traversed. The reasons for the allowability of Claim 1 over the patent to Maemura are set forth above, and Claim 7 depends from Claim 1. The patent to Jaggar fails to cure the deficiencies of the patent to Maemura, apparently relating to debug logic using a JTAG scan chain, and failing to teach or suggest a program counter copy register for storing a program memory address pointed to by a program counter as a return address from a debug monitor routine. In addition, it fails to teach or suggest the additional limitations found in this dependent claim. It is therefore respectfully submitted that Claim 1 is allowable over Maemura and Jaggar. Since Claim 7 depends from Claim 1, it is allowable for the same reasons, as well as for the additional limitations found therein. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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